36V;1.5μA IQ,150mA Low-Dropout Linear Voltage Regulator

Features

- Low Power Consumption: 1.5μA (Typ)
- Maximum Output Current: 150mA
- Small Dropout Voltage
  300mV@100mA (Vout=3.3V)
- High Input Voltage: Up to 36V
- High Accurate:
  CST7550(B)±2% Output Voltage
  CST755 0(A)±1%Output Voltage
- RoHS Compliant and Lead (Pb) Free
- Good Transient Response
- Integrated Short-Circuit Protection
- Over-Temperature Protection
- Output Current Limit
- Stable with Ceramic Capacitor
- Support Fixed Output Voltage
  1.8,2.5,3.0,3.3,3.6,4,0,4.2 and 5.0V
- Available Package
  SOT23-3 \ SOT89-3

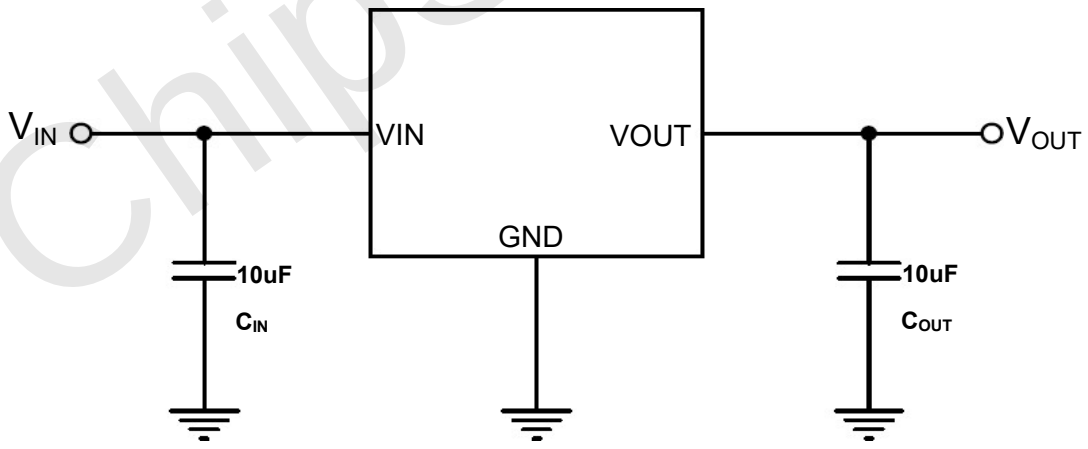
Application

- Portable, Battery Powered Equipment
- Battery-powered equipment
- Weighting Scales
- Smoke detector and sensor
- Audio/Video Equipmen
- Home Automation

Description

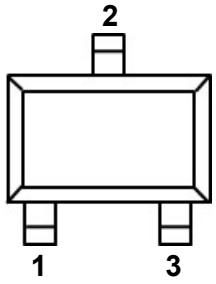
The CST7550 series is a high voltage, ultra low-power, low dropout voltage regulator. The device can deliver 150mA output current with a dropout voltage of 300mV and allows an input voltage as high as 36V. The typical quiescent current is only 1.5μA. The device is available in fixed output voltages of 1.8,2.5,2.8,3.0,3.3,3.6,4.0,4.2,4.4 and 5.0V.The device features integrated short-circuit and thermal shutdown protection.Although designed primarily as fixed voltage regulators, the device can be used with external components to obtain variable voltages.

Application Circuits



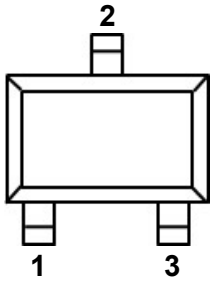
Pin Configuration

SOT23-3L



CST7550S3-XX

SOT23-3L



CST7550SA-XX

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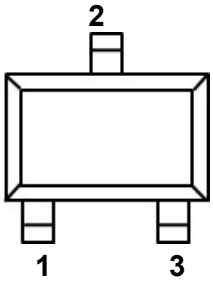

CST7550SB-XX

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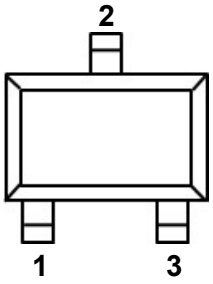

CST7550SC-XX

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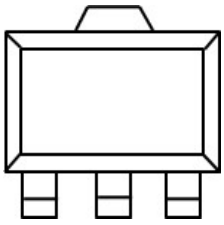
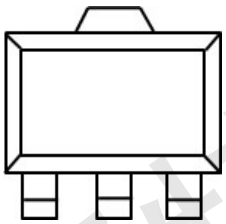


CST7550P3-XX

SOT89-3L



CST7550PA-XX

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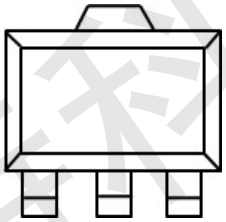

CST7550PB-XX

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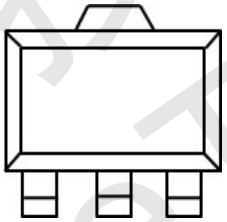


CST7550PC-XX

Pin Description

SOT23-3L Pin No.				Pin Name	Pin Function
CST7550S3-XX	CST7550SA-XX*	CST7550SB-XX*	CST7550SC-XX*		
1	3	2	2	GND	Ground.
2	2	1	3	VIN	Supply voltage input
3	1	3	1	VOUT	Voltage Output
SOT89-3L Pin No.				Pin Name	Pin Function
CST7550P3-XX	CST7550PA-XX*	CST7550PB-XX*	CST7550PC-XX*		
1	3	2	2	GND	Ground.
2	2	1	3	VIN	Supply voltage input
3	1	3	1	VOUT	Voltage Output

NOTE: (*) It needs to be customized

Order Information

CST7550①②-③④⑤

Designator	Symbol	Description
①②	S3/P3	SOT23-3L / SOT89-3L
③④	Integer	Output Voltage 1.8,2.5,2.8.3.0,3.3,3.6,4.0,4.2 and 5.0V
⑤	A	Accurate ±1%
	B	Accurate ±2%

Model	Marking	Description	Package	T/R Qty
CST7550S3-XX*	AFXXA(B)	CST7550 36V;1.5μAIQ 150mA Low-Dropout LDO	SOT23-3L	3,000 PCS
CST7550P3-XX*	AFXXA(B)		SOT89-3L	1,000 PCS

Note：(*) XX Represents the Output Voltage

Marking Information ①②③④⑤

①②Represents the product name

Mark ①②	Product Series
AF	CST7550 S3/P3

③④Represents the Output Voltage

Mark	Output Voltage (V)			Mark	Output Voltage (V)		
18	——	1.8	——	36	——	3.6	——
25	——	2.5	——	40	——	4.0	——
28	——	2.8	——	42	——	4.2	——
30	——	3.0	——	50	——	5.0	——
33	——	3.3	——	——	——	——	——

⑤Represents the Output Voltage Accurate

Mark⑤		Product Series
±1% Output Voltage	±2% Output Voltage	CST7550(AorB)
A	B	

Absolute Maximum Ratings (1) (2)

Parameter		Symbol	Maximum Rating	Unit
Input Voltage		V_{IN}	V_{SS} -0.3~V_{SS}+42.0	V
		V_{OUT}	V_{SS} -0.3~V_{SS}+6.0	V
Output Current		I_{OUT}	150	mA
Power Dissipation	SOT23-3	Pd	400	mW
	SOT89-3		500	
Thermal Resistance	SOT23-3	$R_{\theta JA}$ (3)	250	℃/W
	SOT89-3		200	℃/W
Operating Temperature		Topr	-40~85	℃
Storage Temperature		Tstg	-40~125	℃
Soldering Temperature & Time		Tsolder	260℃, 10s	

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions

Note (3): The package thermal impedance is calculated in accordance to JESD 51-7.

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±4000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±100	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

ESD testing is performed according to the respective JESD22 JEDEC standard.The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Recommended Operating Conditions

Parameter	MIN.	MAX.	Units
Supply voltage at V_{IN}	3.0	24	V
Operating junction temperature range, Tj	-40	125	°C
Operating free air temperature range, TA	-40	85	°C

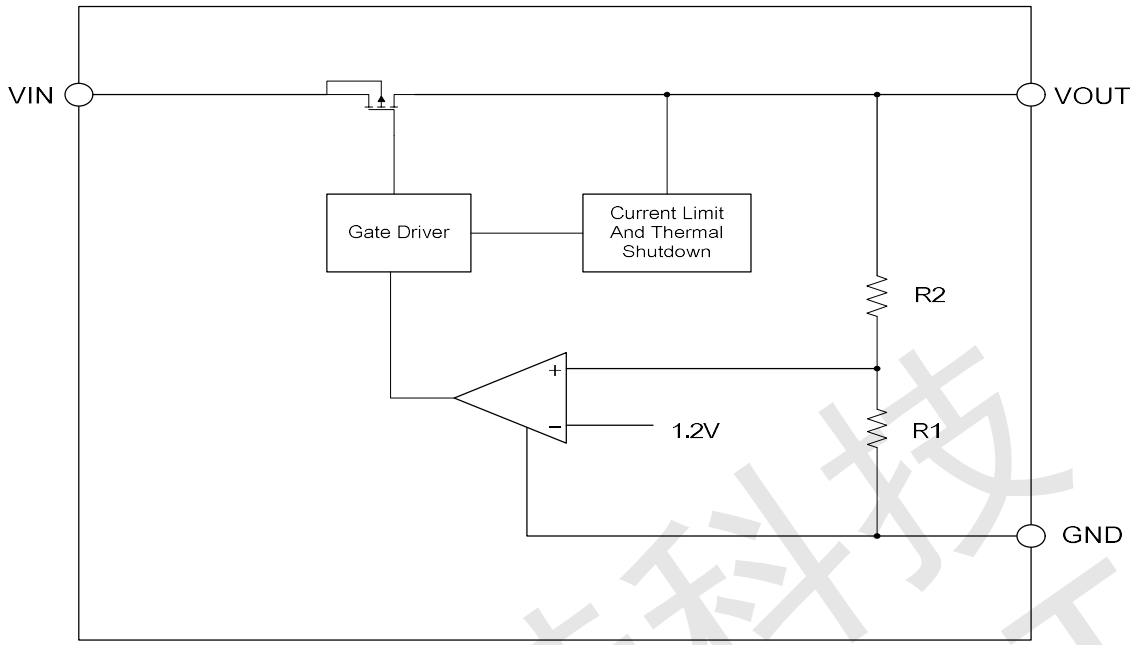
Note : All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

(Test Conditions:V_{IN}=12V, V_{OUT}=Vset,C_{IN}=10uF, C_{OUT}=10uF,TA=25℃, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage	V_{IN}		3.0	—	36	V
Supply Current	I_Q	V_{IN}=12V I_{LOAD}=0mA	—	1.5	3.0	uA
Output Voltage CST7550 (A)	V_{OUT1}	V_{IN}=12V I_{OUT}=10mA	Vset*0.99	Vset	Vset*1.01	V
Output Voltage CST7550 (B)	V_{OUT2}	V_{IN}=12V I_{OUT}=10mA	Vset*0.98	Vset	Vset*1.02	V
Maximum Output Current	I_{OUT}(Max)	—	—	150	—	mA
Dropout Voltage	V_{DROP} V_{OUT}=3.0V	I_{OUT}=150mA	—	550	—	mV
		I_{OUT}=100mA	—	330	—	
	V_{DROP} V_{OUT}=3.3V	I_{OUT}=150mA	—	500	—	
		I_{OUT}=100mA	—	300	—	
	V_{DROP} V_{OUT}=5.0V	I_{OUT}=150mA	—	520	—	
		I_{OUT}=100mA	—	300	—	
Line Regulation	ΔV_{OUT}/ $\Delta V_{IN} \cdot V_{OUT}$	I_{OUT}=10mA (Vset+2.0v)≦V_{IN}≦24V	—	0.15	—	%/V
Load Regulation	ΔV_{OUT}	V_{IN}=10V 1mA≦I_{OUT}≦150mA	—	45	—	mV
Short Current	I_{SHORT}	RL=1Ω	—	80	—	mA
Output Noise Voltage	e_{NO}	I_{OUT}=50mA BW = 300Hz~50kHz	—	50	—	uV_{RMS}
Output Voltage Temperature Coefficient	ΔV_{OUT}/ $\Delta T \cdot V_{OUT}$	I_{OUT}=10mA	—	100	—	ppm/℃

Function Block Diagram



Application Guideline

Input Capacitor

A 10μF ceramic capacitor is recommended to connect between V_{DD} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is 10μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage VDROP also can be expressed as the voltage drop on the pass-FET at specific output current (IRATED) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized asan resistance RDS(ON). Thus the dropout voltage can bedefined as (VDROP = VIN − VOUT = RDS(ON) x IRATED). Fornormal operation, the

suggested LDO operating range is (VIN > VOUT + VDROP) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below: TA=25°C, PCB,

The max PD= (125°C − 25°C) / (Thermal Resistance °C/W)

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

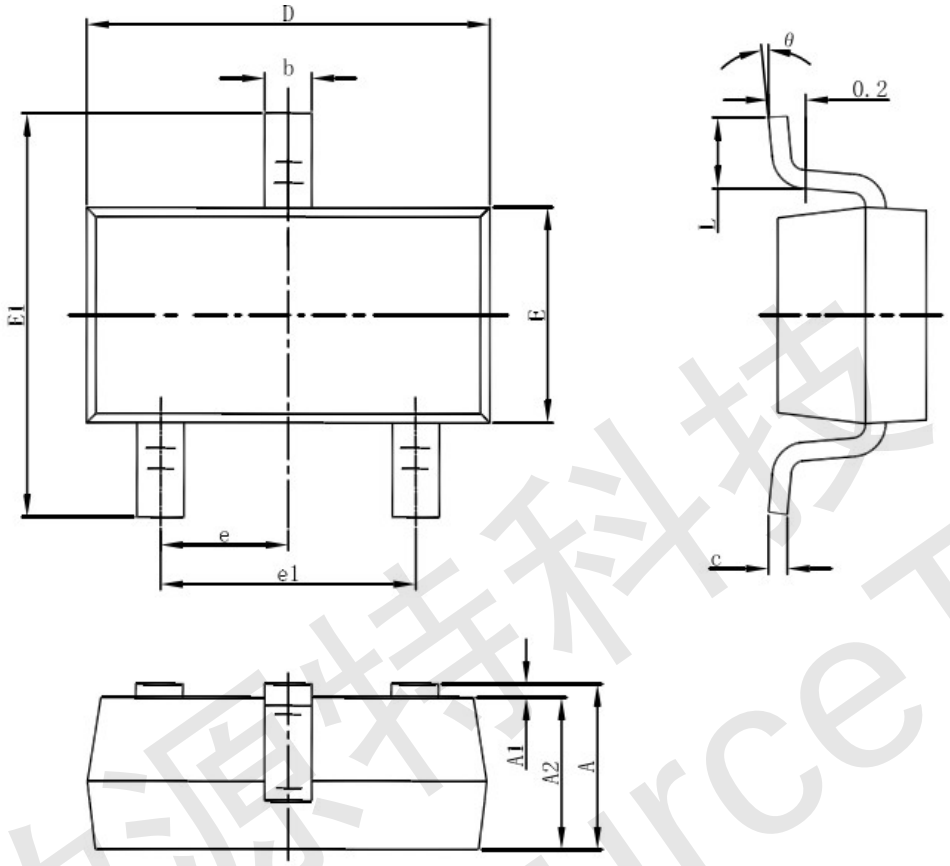
PD = (VIN – VOUT) × IOUT

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the CST7550 ground pin using as wide and short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Packaging Information

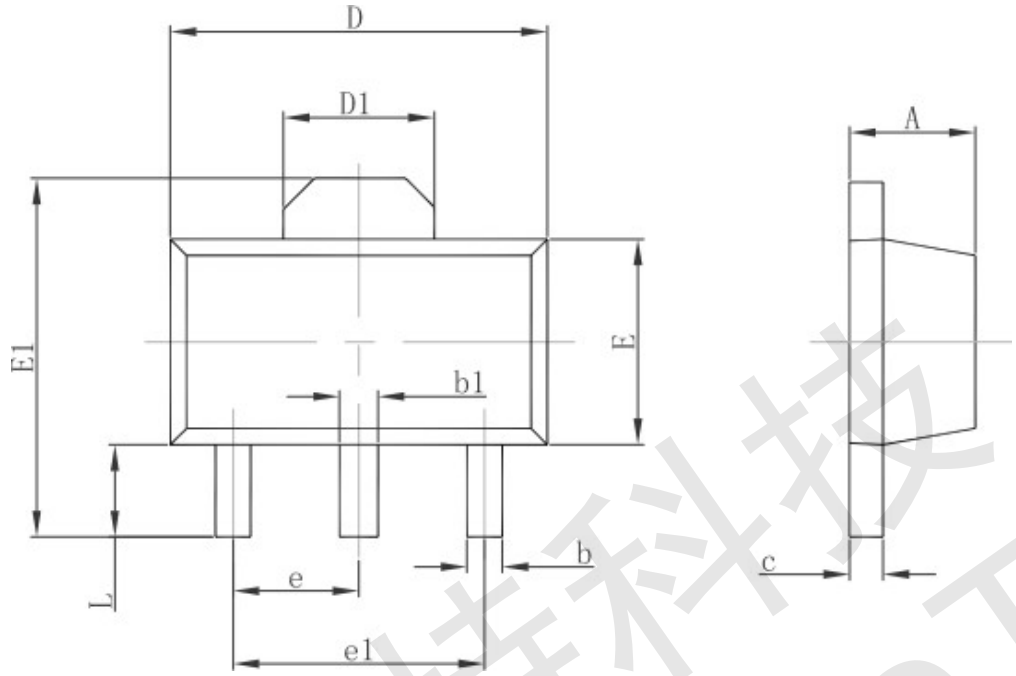
SOT23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Packaging Information

SOT89-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047